

Notice of References Cited

Application/Control No.

09/273,560

Applicant(s)/Patent Under
Reexamination
HASEGAWA, TAKUMI

Examiner

Kandasamy Thangavelu

Art Unit

2123

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U.S. PATENT DOCUMENTS

*		Document Number	Date	Name	Classification	
		Country Code-Number-Kind Code	MM-YYYY			
	A	US-5,274,568	12-1993	Blinne	716	6
	B	US-4,698,760	10-1987	Lembach	716	6
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number	Date	Country	Name	Classification	
		Country Code-Number-Kind Code	MM-YYYY				
	N						
	O						
	P						
	Q						
	R						
	S						
	T						

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages					
	U	Jun, et al. "An accurate and efficient multidelay simulator for MOS Logic Circuits Using Polynomial Approximation", IEEE International Symposium on Circuits and Systems, 1988, Pages 2117-2120.					
	V	Edmatsu et al. " Pre-layout calculation specification for CMOS ASIC Libraries", Proceedings of the Asia Pacific Design Automation Conference, Feb 1998, Pages 241-248.					
	W	Pratapneni, et al. " Comparison of driver models for the computer aided analysis of Electronic packages", Electircal Performance and Electronic Packaging, Oct 1993, Pages 199-201.					
	X						

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.